

General Description

The G110N06T is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged E_{AS} capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching applications.

Features

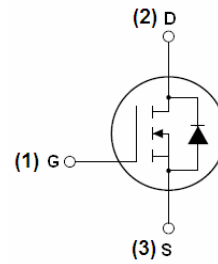
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V_{DS}	$R_{DS(ON)}$ @10V(Typ)	I_D
60V	5.2 mΩ	110A

- Ultra Low On-Resistance
- High UIS and UIS 100%Test
- RoHS Compliant

Application

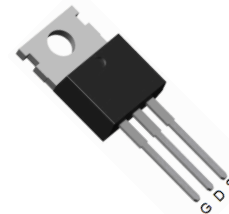
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic diagram



Marking and pin assignment



TO-220

Ordering Information

Part Number	Marking	Case	Packaging
G110N06T	G110N06	TO-220	50pcs/Tube

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	60	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	±20	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	110	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	65	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	368	A
dv/dt	Peak Diode Recovery Voltage	30	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	120	W
	Derating Factor	0.8	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	440	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. E_{AS} condition: $T_J=25^\circ C, V_{DD}=33V, V_G=10V, I_D=45A$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.25	$^{\circ}\text{C/W}$

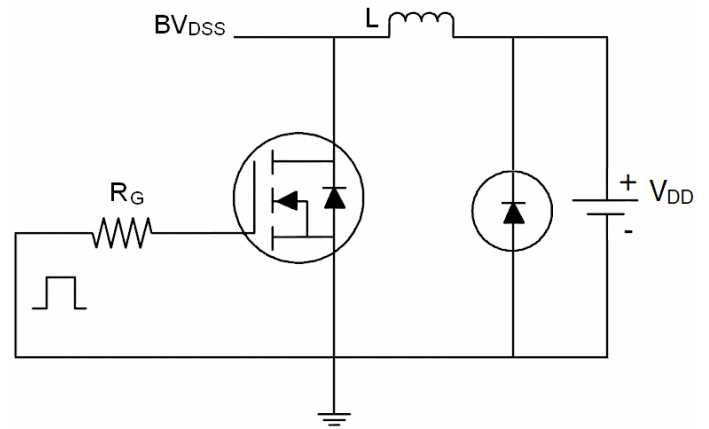
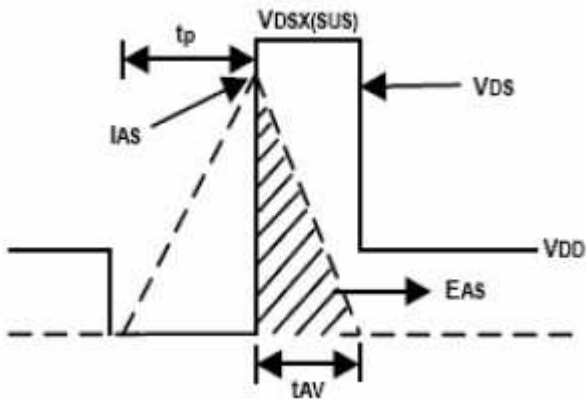
Table 3. Electrical Characteristics (TA=25 $^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	60			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V _{DS} =60V,V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=125℃)	V _{DS} =60V,V _{GS} =0V			10	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	1	1.5	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =20A		5.2	6.4	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =4.5V, I _D =20A		6.2	8.4	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V,I _D =15A	20			S
C _{iss}	Input Capacitance	V _{DS} =25V,V _{GS} =0V, f=1.0MHz		5538		pF
C _{oss}	Output Capacitance			380		pF
C _{rss}	Reverse Transfer Capacitance			304		pF
Q _g	Total Gate Charge	V _{DS} =50V,I _D =40A, V _{GS} =10V		113		nC
Q _{gs}	Gate-Source Charge			14		nC
Q _{gd}	Gate-Drain Charge			54		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V,I _D =2A,R _L =15Ω V _{GS} =10V,R _G =2.5Ω		13		nS
t _r	Turn-on Rise Time			15		nS
t _{d(off)}	Turn-Off Delay Time			27		nS
t _f	Turn-Off Fall Time			32		nS
Source-Drain Diode Characteristics						
I _{SD}	Source -Drain Current (Body Diode)			110		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			368		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25℃,I _{SD} =20A,V _{GS} =0V		0.7	1.2	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25℃,I _F =75A di/dt=100A/μs		49		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			97		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

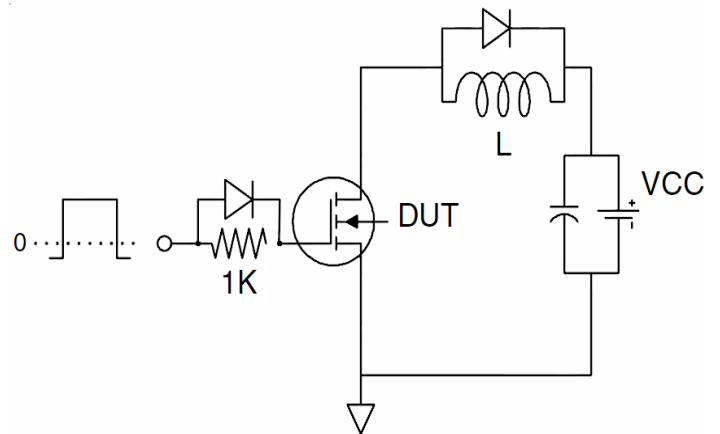
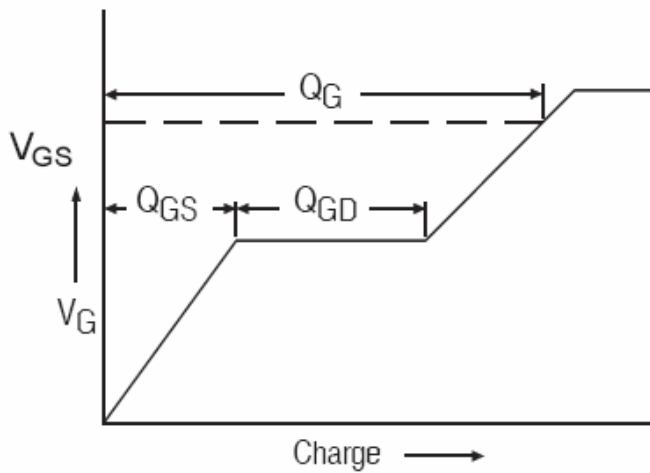
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

Test Circuit

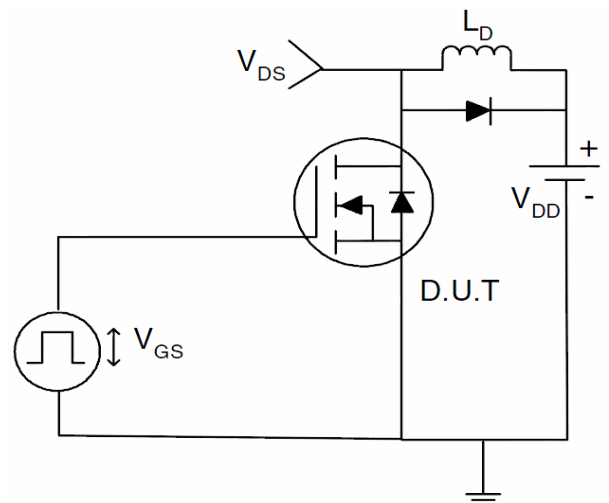
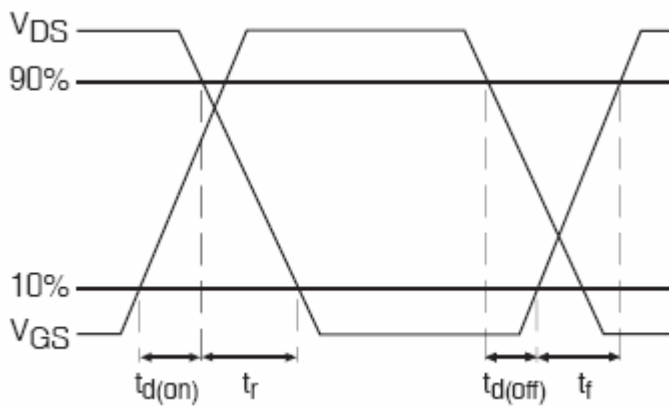
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Safe Operating Area

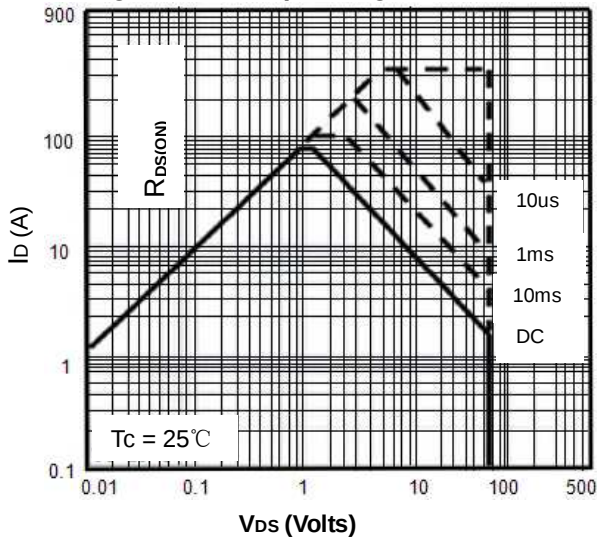


Figure2. Source-Drain Diode Forward Voltage

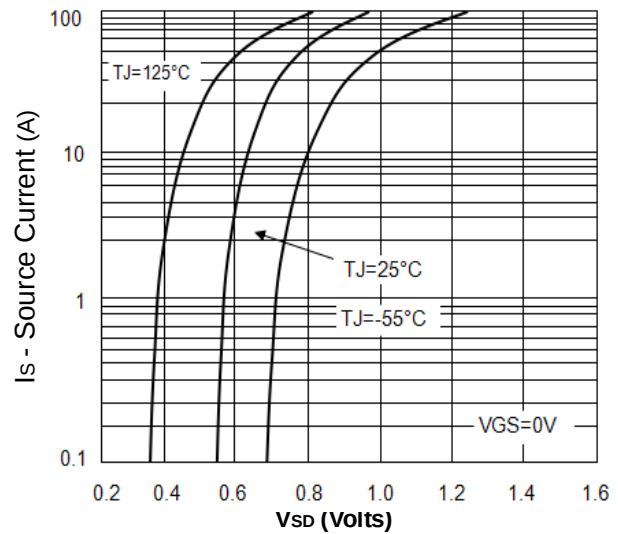


Figure3. Output Characteristics

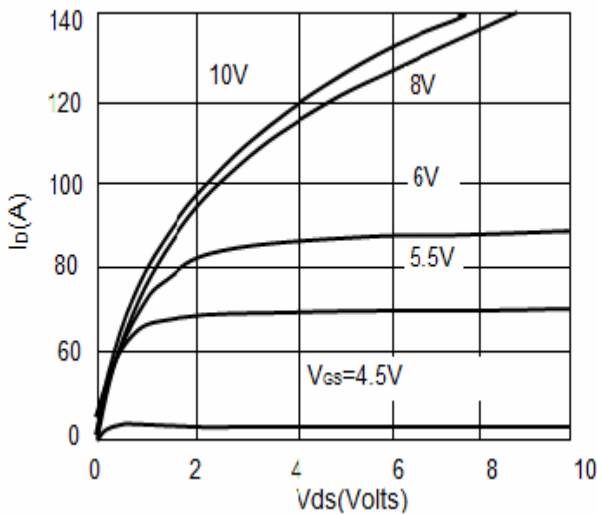


Figure4. Transfer Characteristics

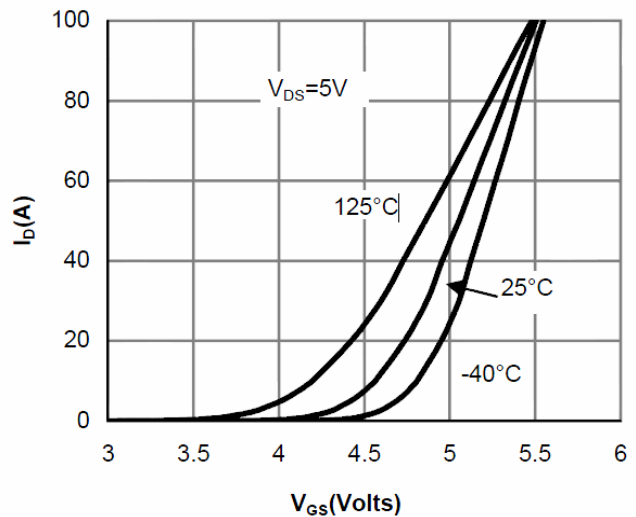


Figure5. Static Drain-Source On Resistance

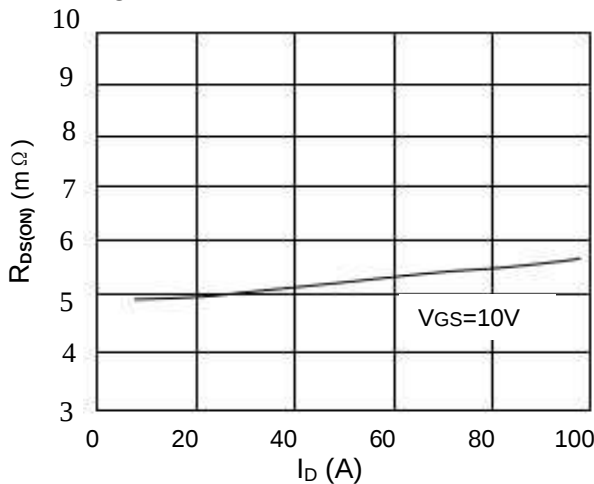


Figure6. $R_{DS(ON)}$ vs Junction Temperature

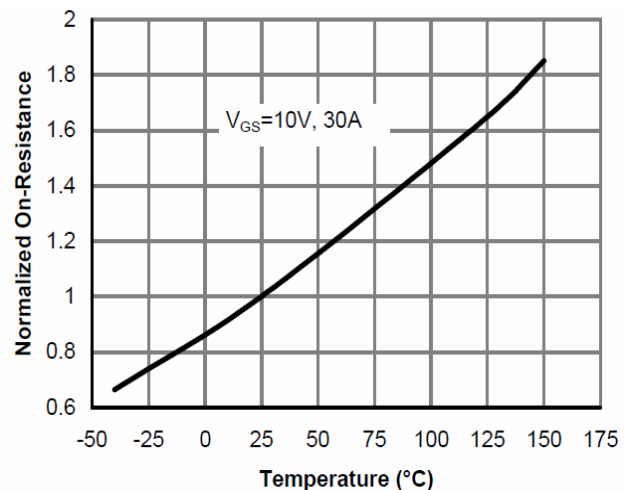
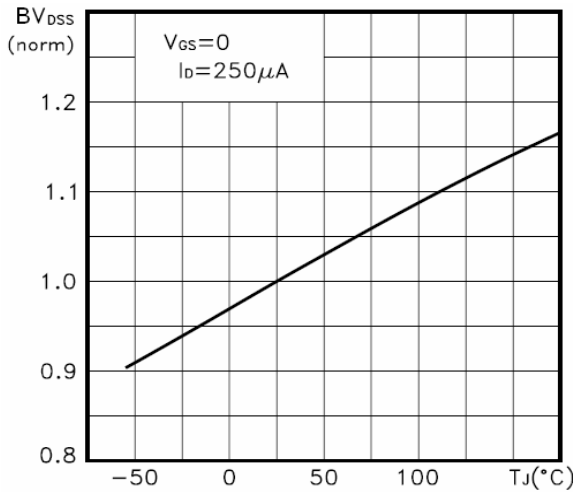
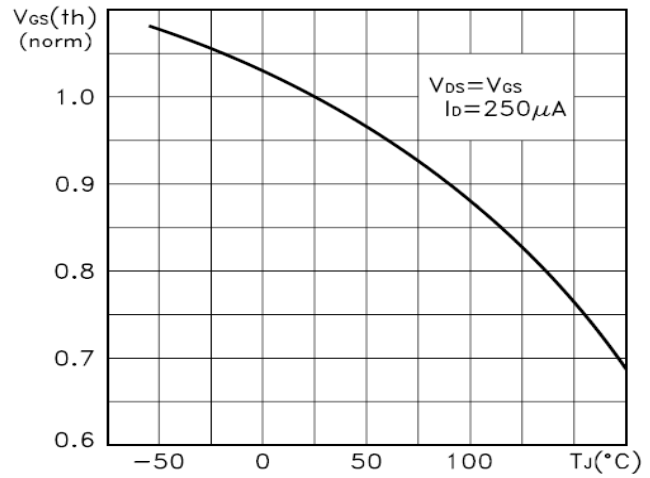


Figure7. BV_{DSS} vs Junction Temperature



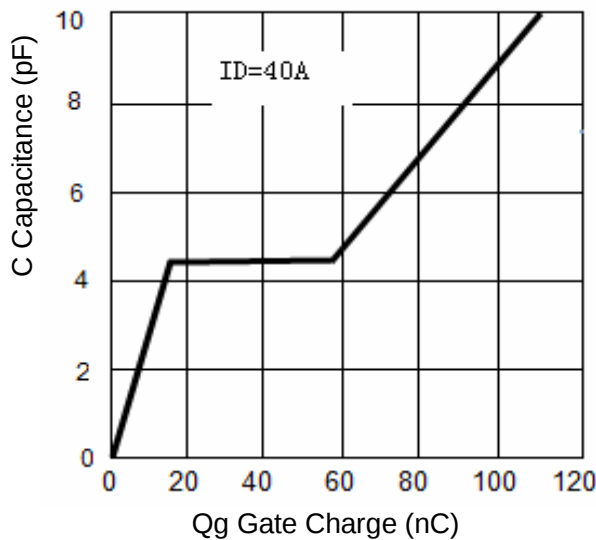
Temperature (°C)

Figure8. $V_{GS(th)}$ vs Junction Temperature



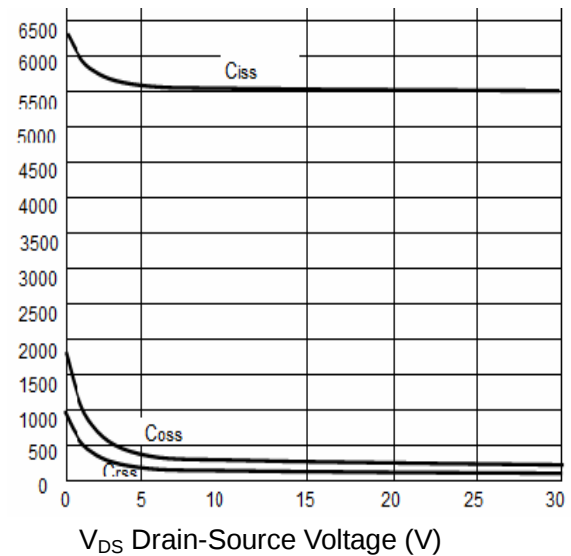
Temperature (°C)

Figure9. Gate Charge Waveforms



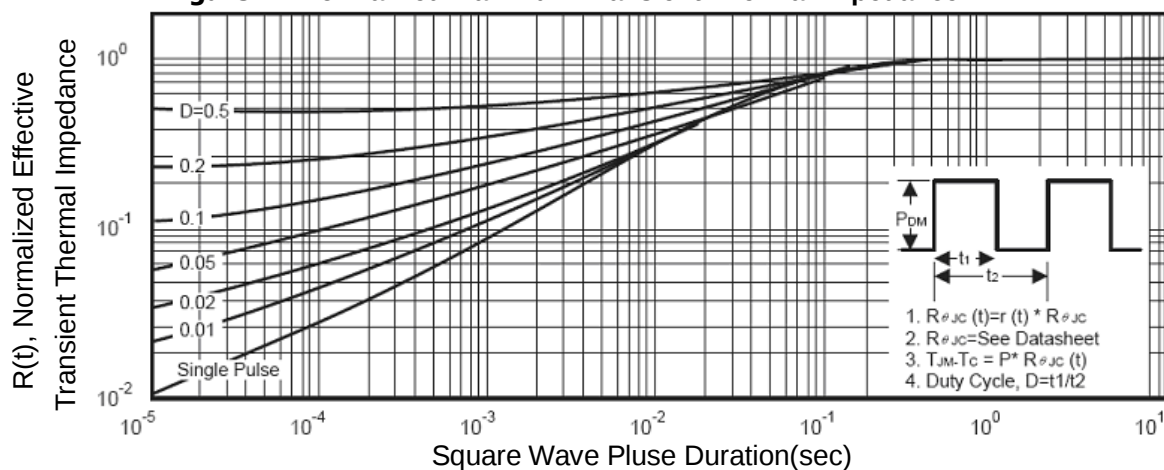
Qg Gate Charge (nC)

Figure10. Capacitance

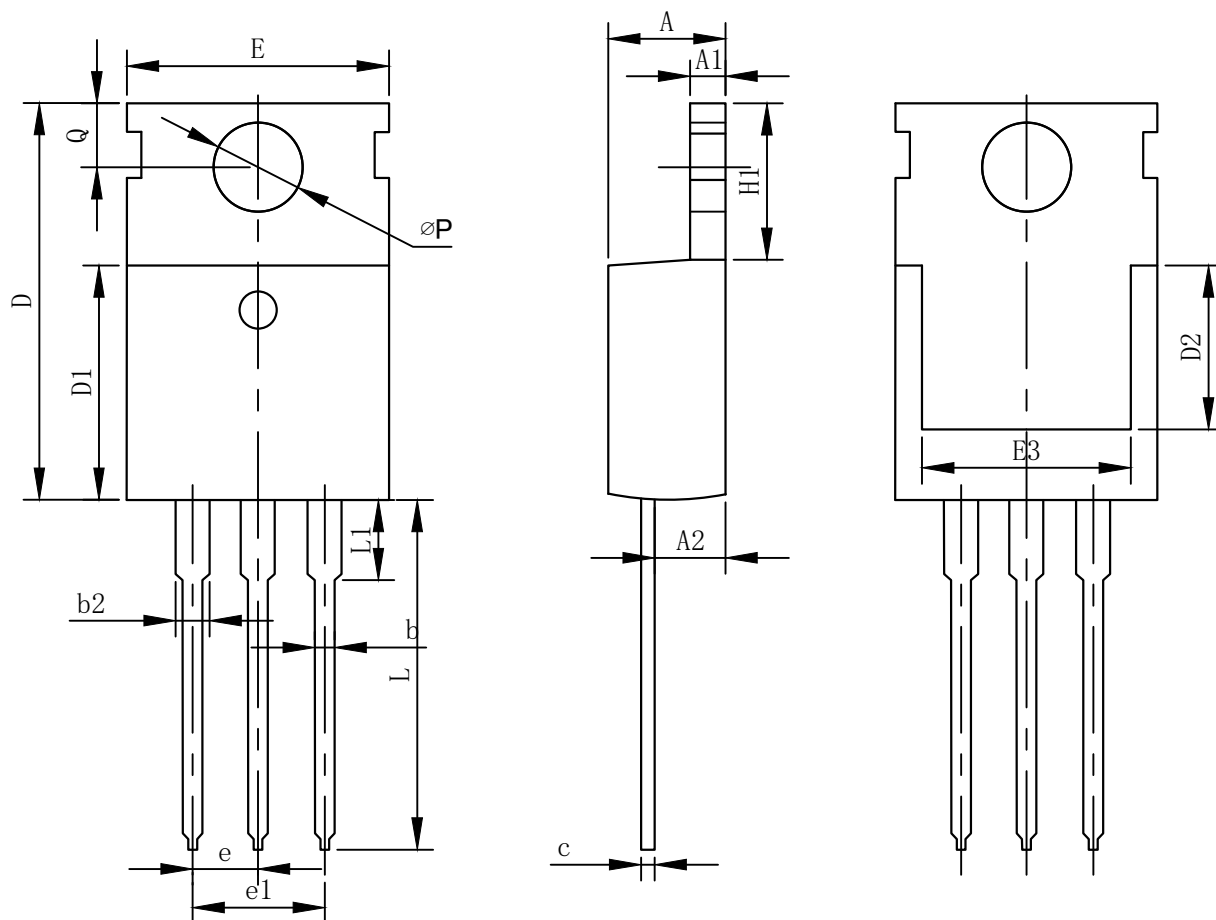


V_{DS} Drain-Source Voltage (V)

Figure11. Normalized Maximum Transient Thermal Impedance



TO-220 Package information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	4.37	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.70	1.27	1.47
c	0.45	0.50	0.60
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	—	—
E	9.70	10.00	10.30
E3	7.00	—	—
e	2.54BSC		
e1	5.08BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	—	3.10	3.40
øP	3.40	3.60	3.80
Q	2.60	2.80	3.00